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Atty. Dkt. No. 016907-1569

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Hiroshi WATANABE et al.  
Title: TIME LIMIT FUNCTION  
UTILIZATION APPARATUS  
Appl. No.: 10/612,405  
Filing Date: 7/3/2003  
Examiner: Vincent Q. Nguyen  
Art Unit: 2858

**STATEMENT OF SUBSTANCE OF INTERVIEW**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In accordance to 37 C.F.R. § 1.133, submitted herewith is a record of the substance of the interview on December 21, 2005, between Examiner Vincent Q. Nguyen and Applicants' representative, Thomas Bilodeau (Reg. No. 43,438), regarding the above-captioned application. This statement is being submitted within one (1) month of the mailing date of December 21, 2005, of the Interview Summary and is therefore a timely response.


Applicants appreciate the courtesies extended by Examiner Nguyen in the interview of December 21, 2005, the Interview Summary of which is of record in this application. Applicants argued with respect to claim 1 that the Lancaster reference does not disclose a semiconductor time switch that substantially disables or enables mutual access between functional blocks. Applicants understand Examiner Nguyen to be of the opinion that Lancaster does disclose this feature in col. 2, lines 25-28 with respect to a memory refresh operation, because the Examiner believes that the phrase "substantially disables or enables mutual access" is broad enough to encompass Lancaster.

Applicants also discussed dependent claims 11-13 with the Examiner, and pointed out that charge is not stored in the gate electrode in the Lancaster device. Applicants understand Examiner Nguyen to be of the opinion that applying a voltage to a gate of a conventional FET would supply charge to the conducting part of the electrode, and that a FET under such an application of voltage would fall within the scope of claim 11.

Respectfully submitted,

Date January 23, 2006

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